

FIG. 1

Dashboard Example

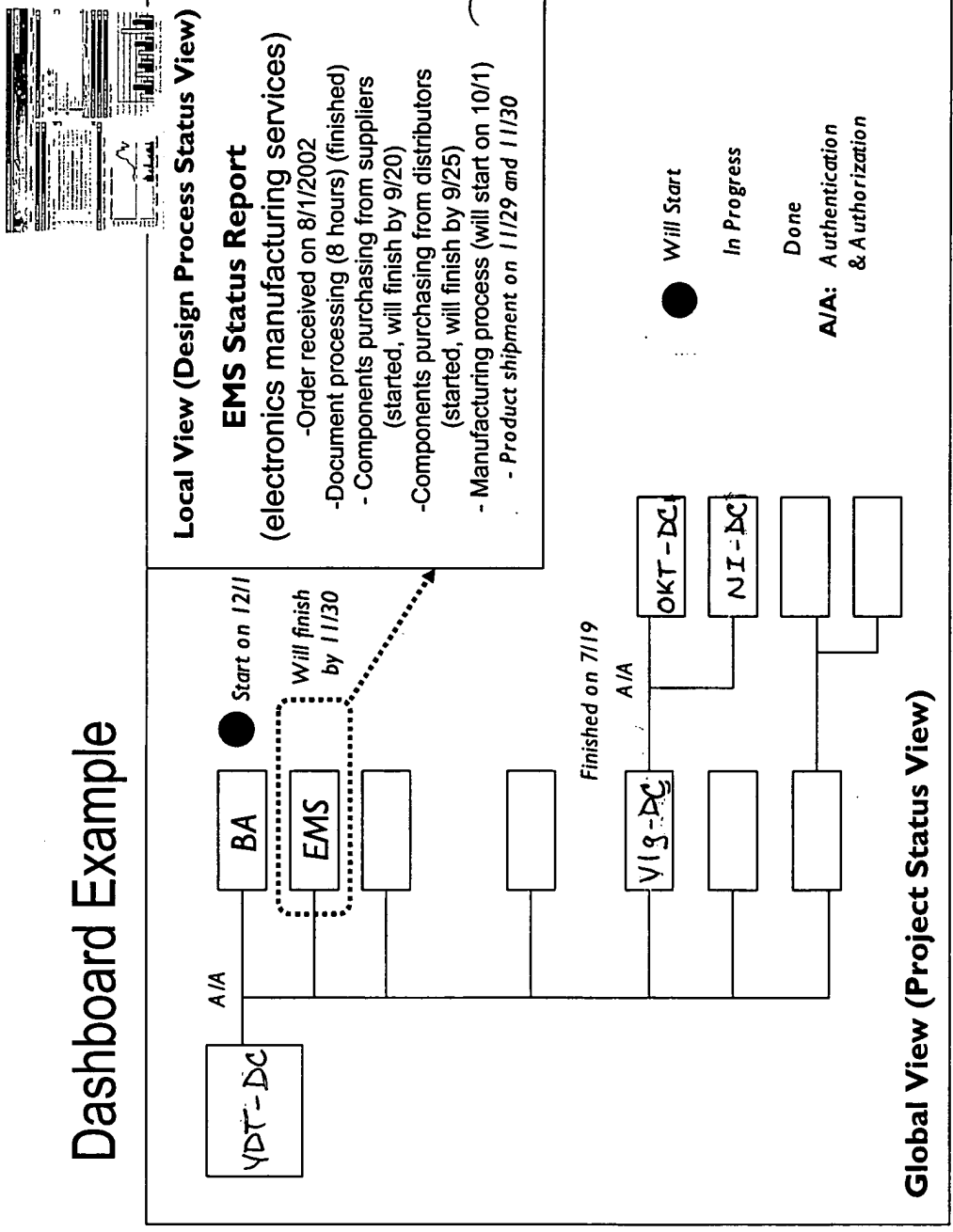
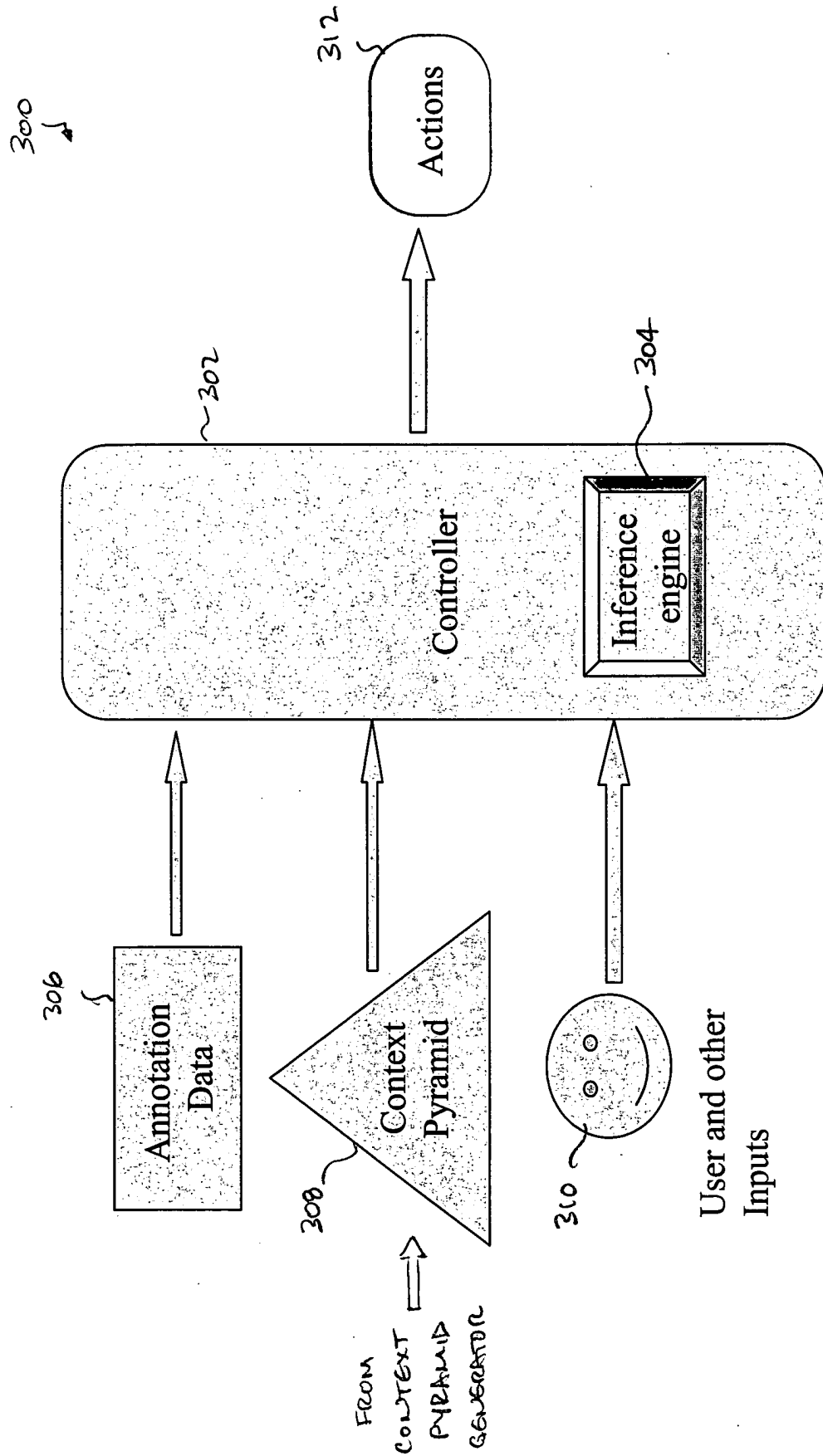
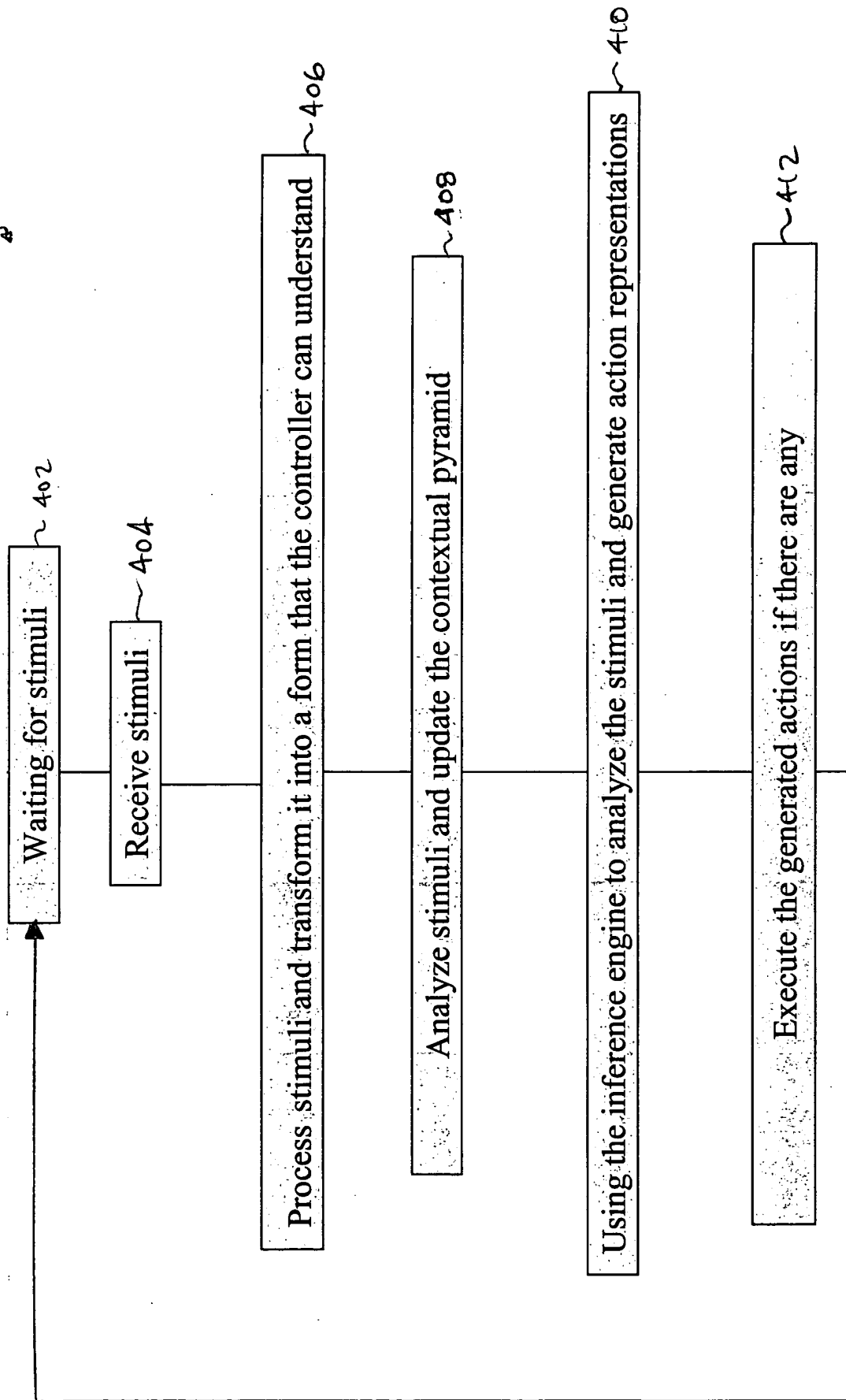


FIG. 2

FIG. 3



400



4(24

FIG. 4

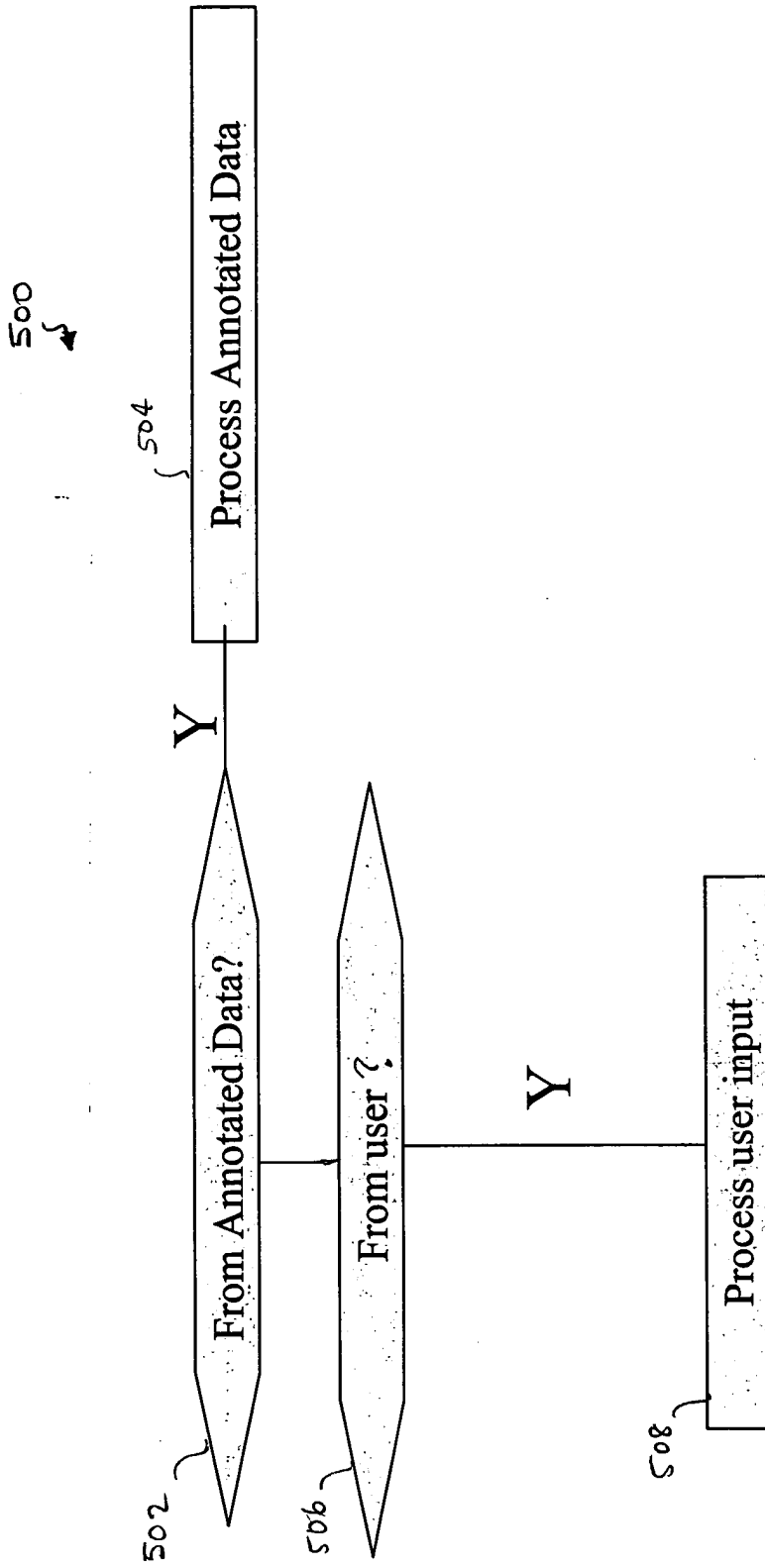


FIG. 5

600

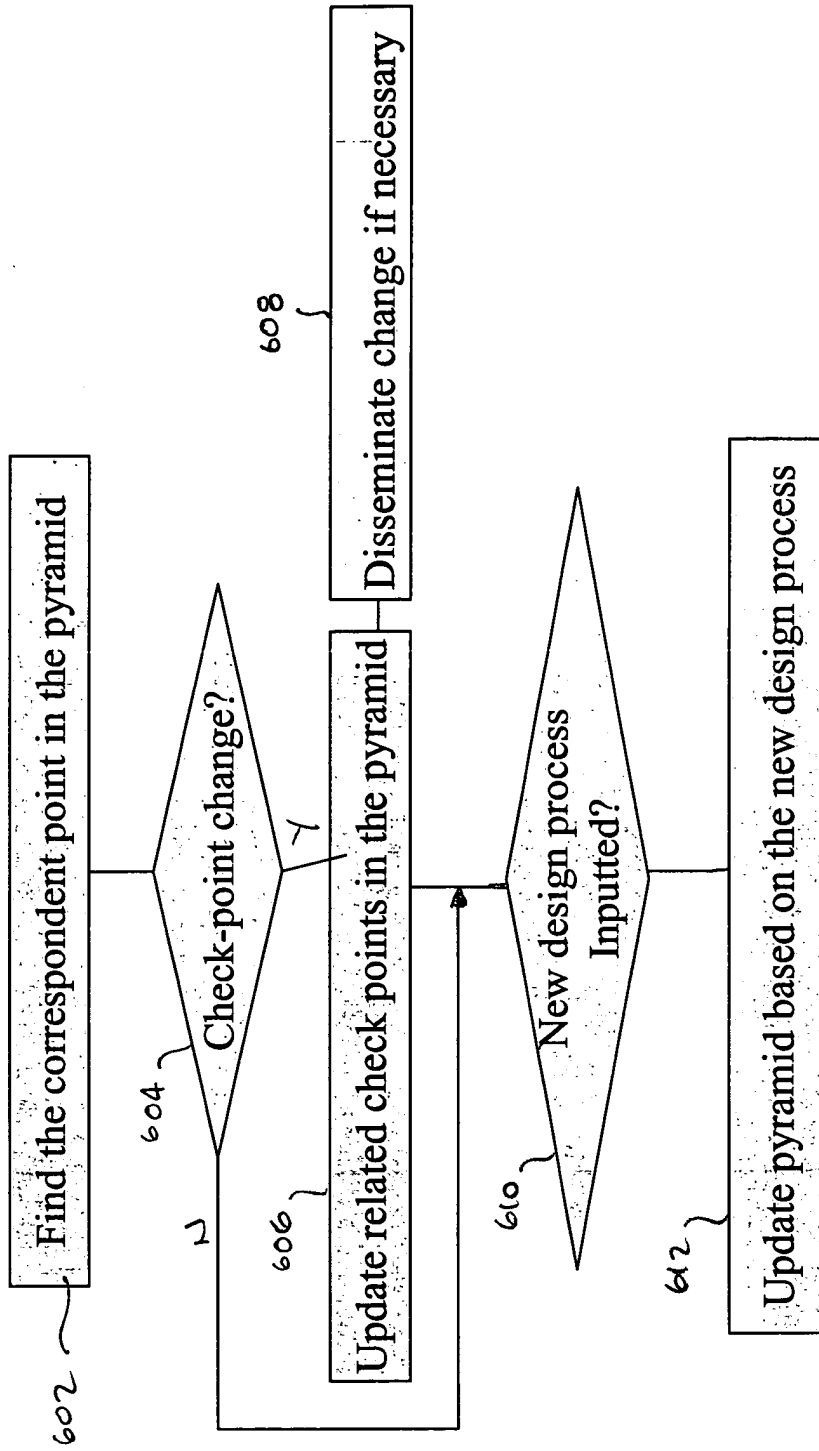


FIG. 6

700

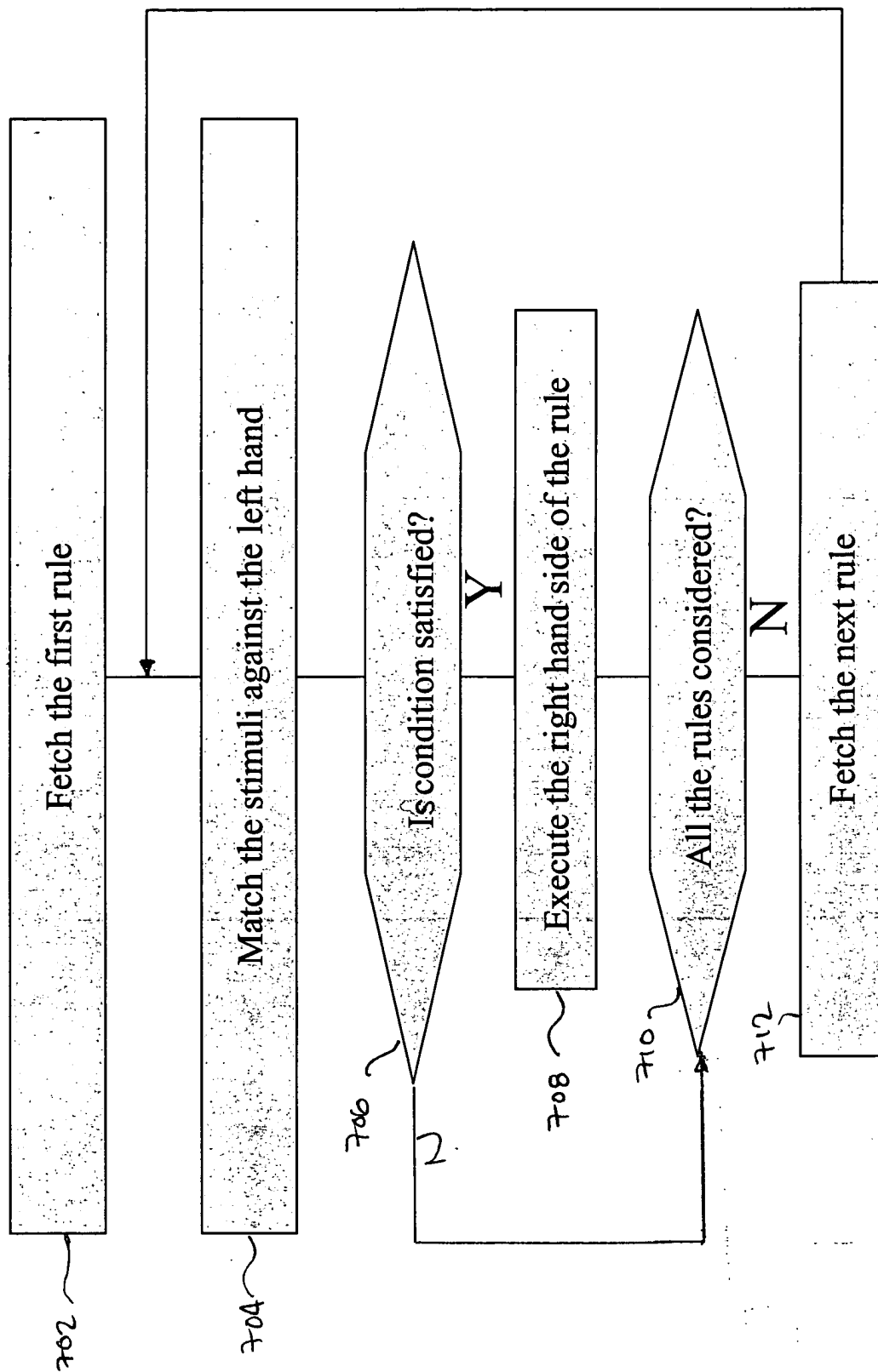


FIG. 7

Fig. 8

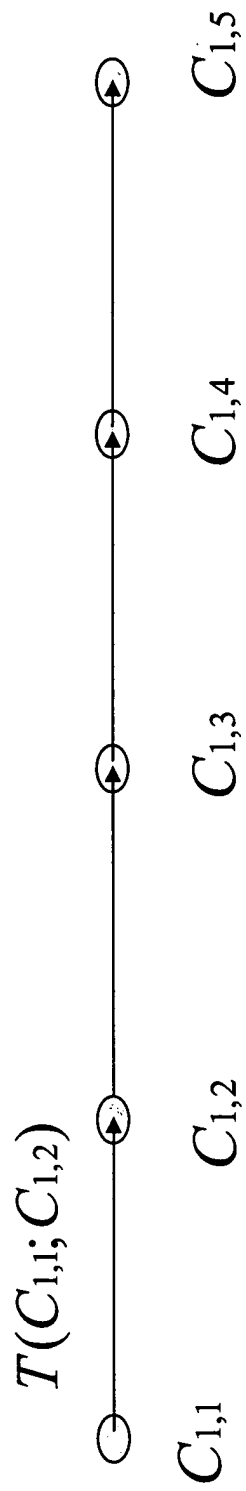


FIG. 9

9/24

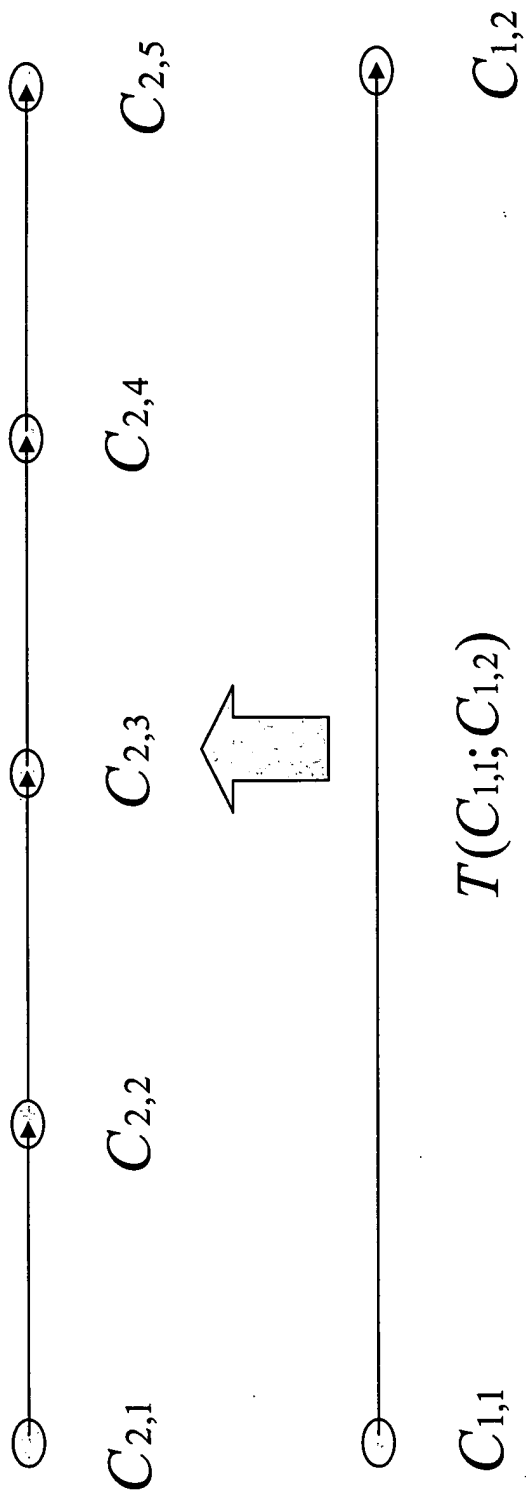
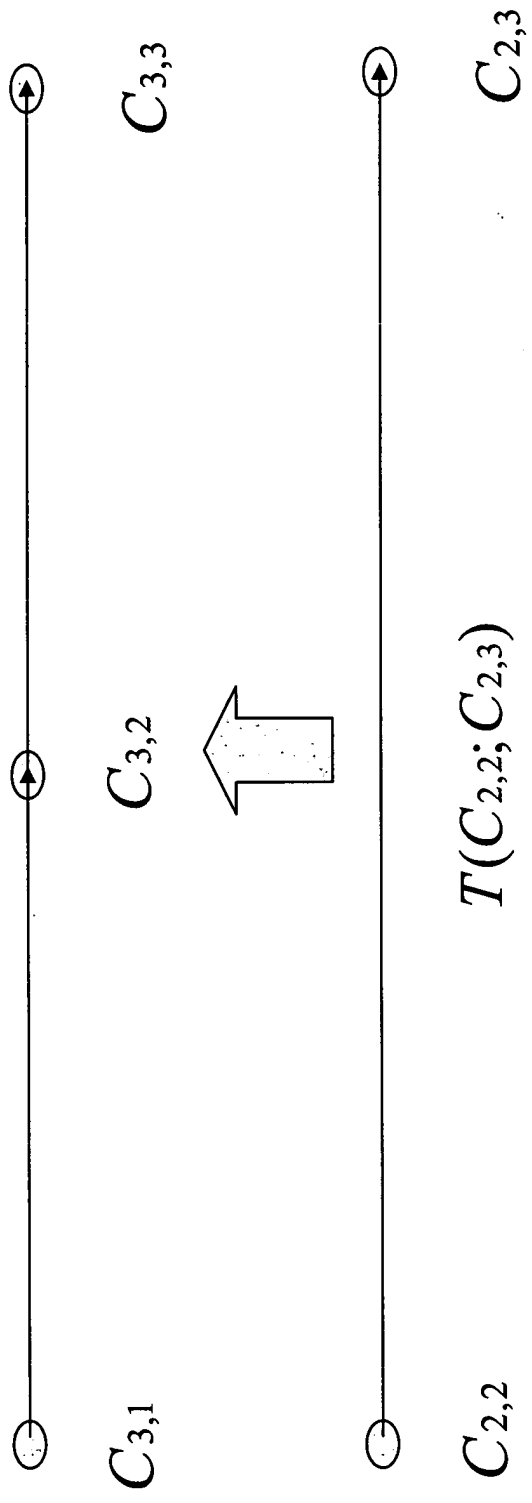


FIG. 10



12/24

FIG. 12

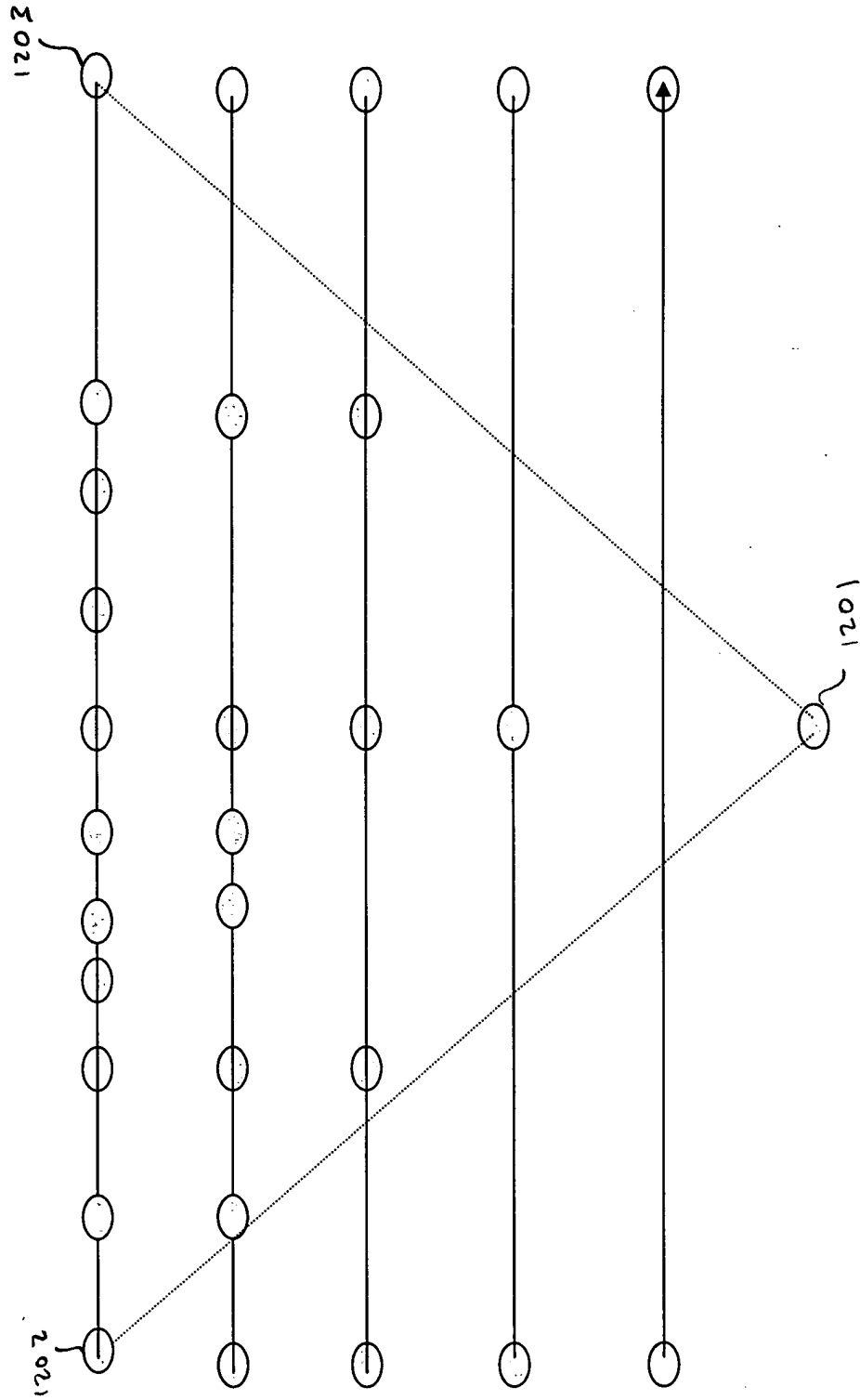


FIG. 13

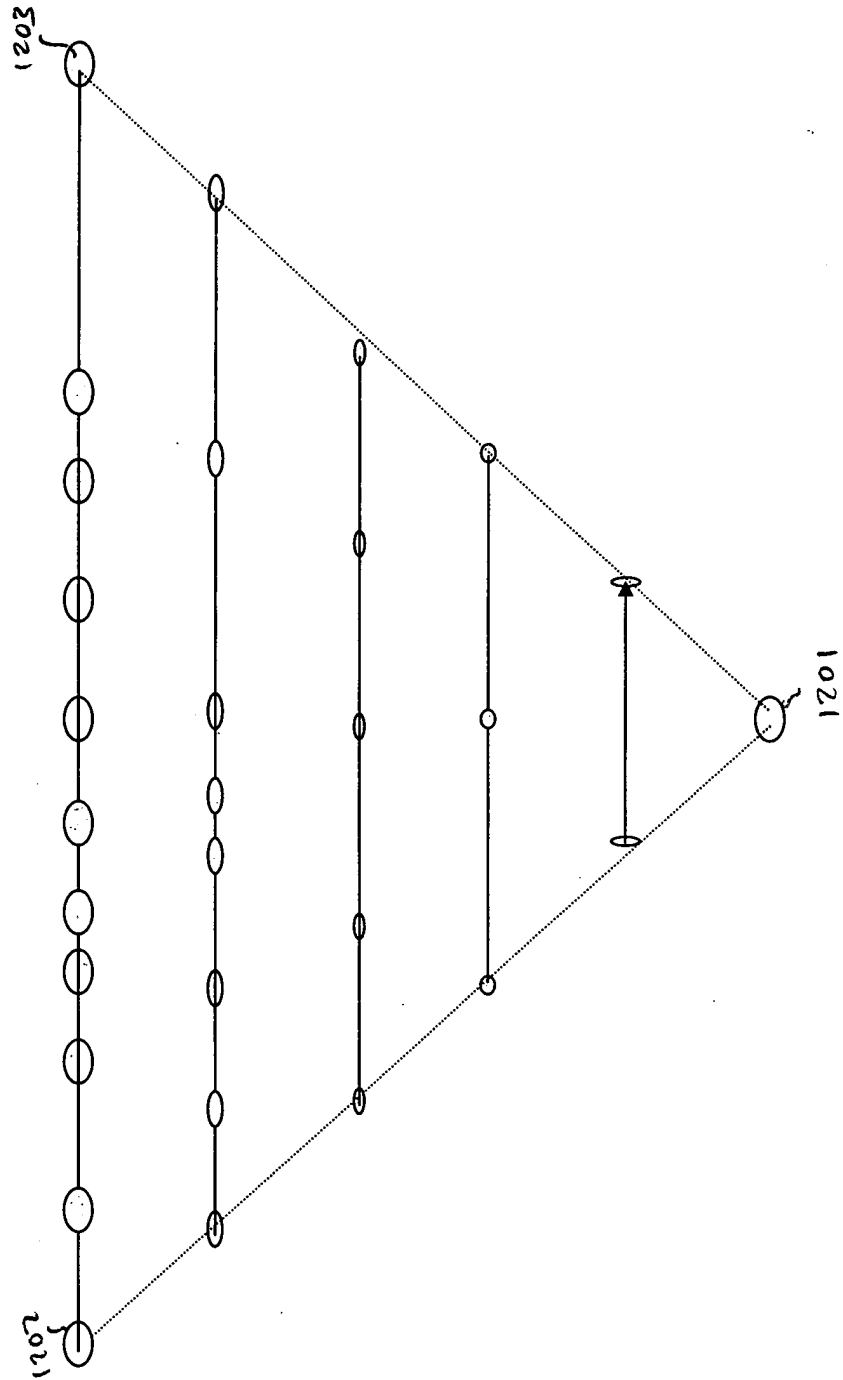


FIG. 14

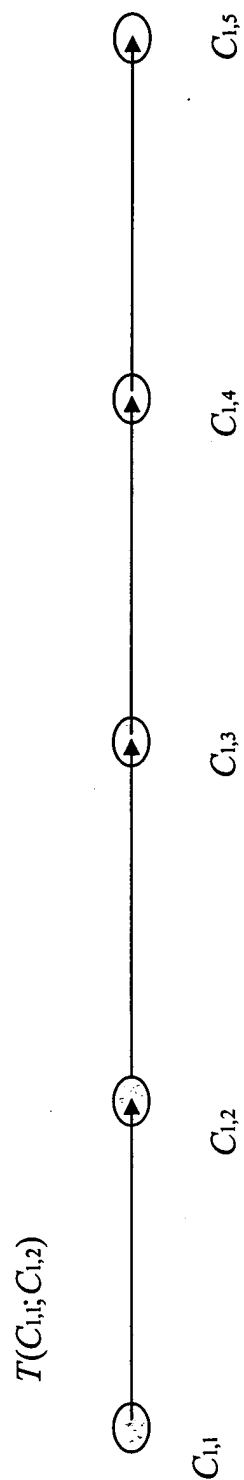
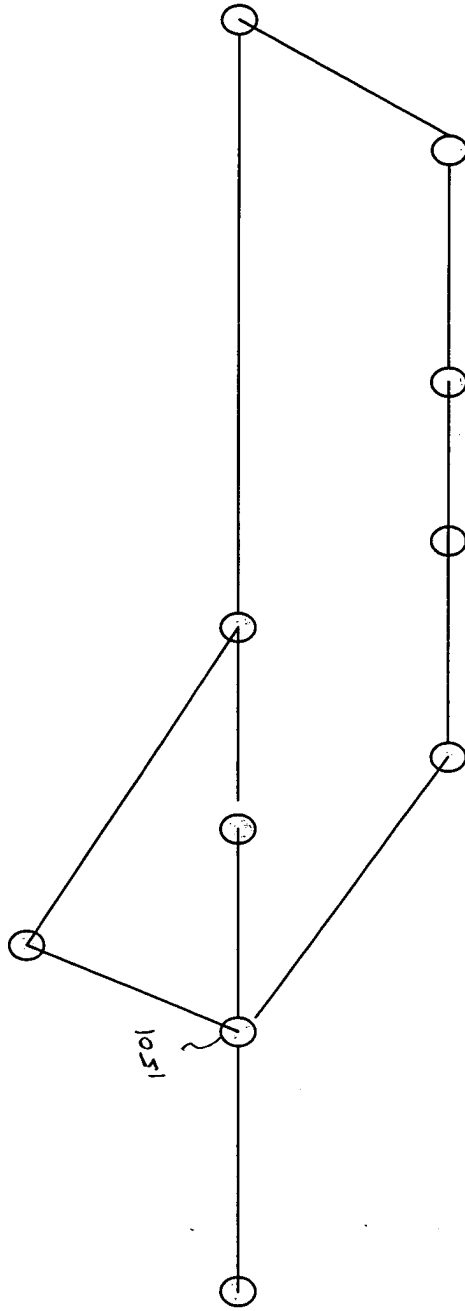


FIG. 15



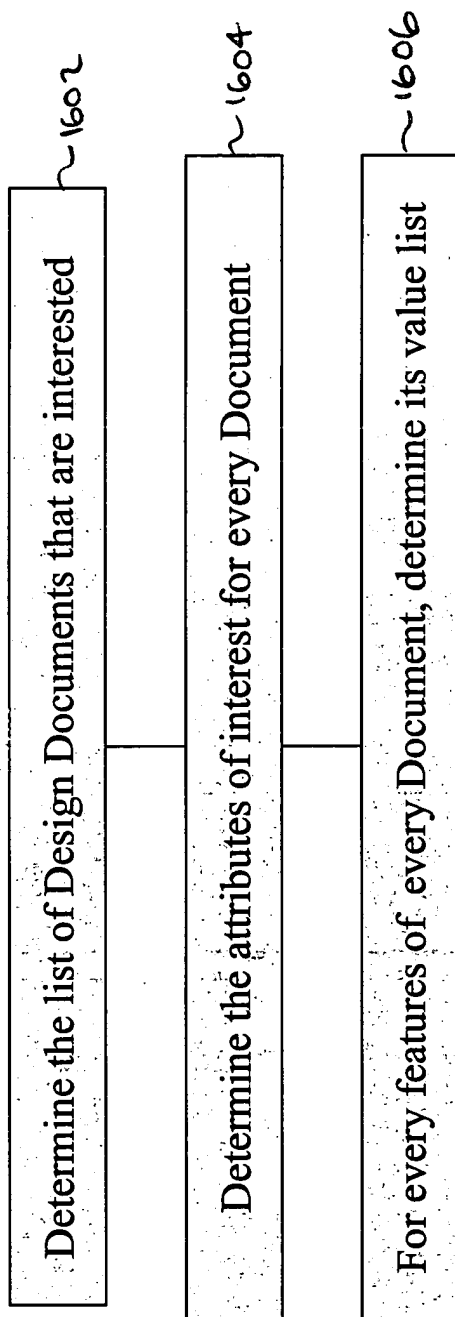
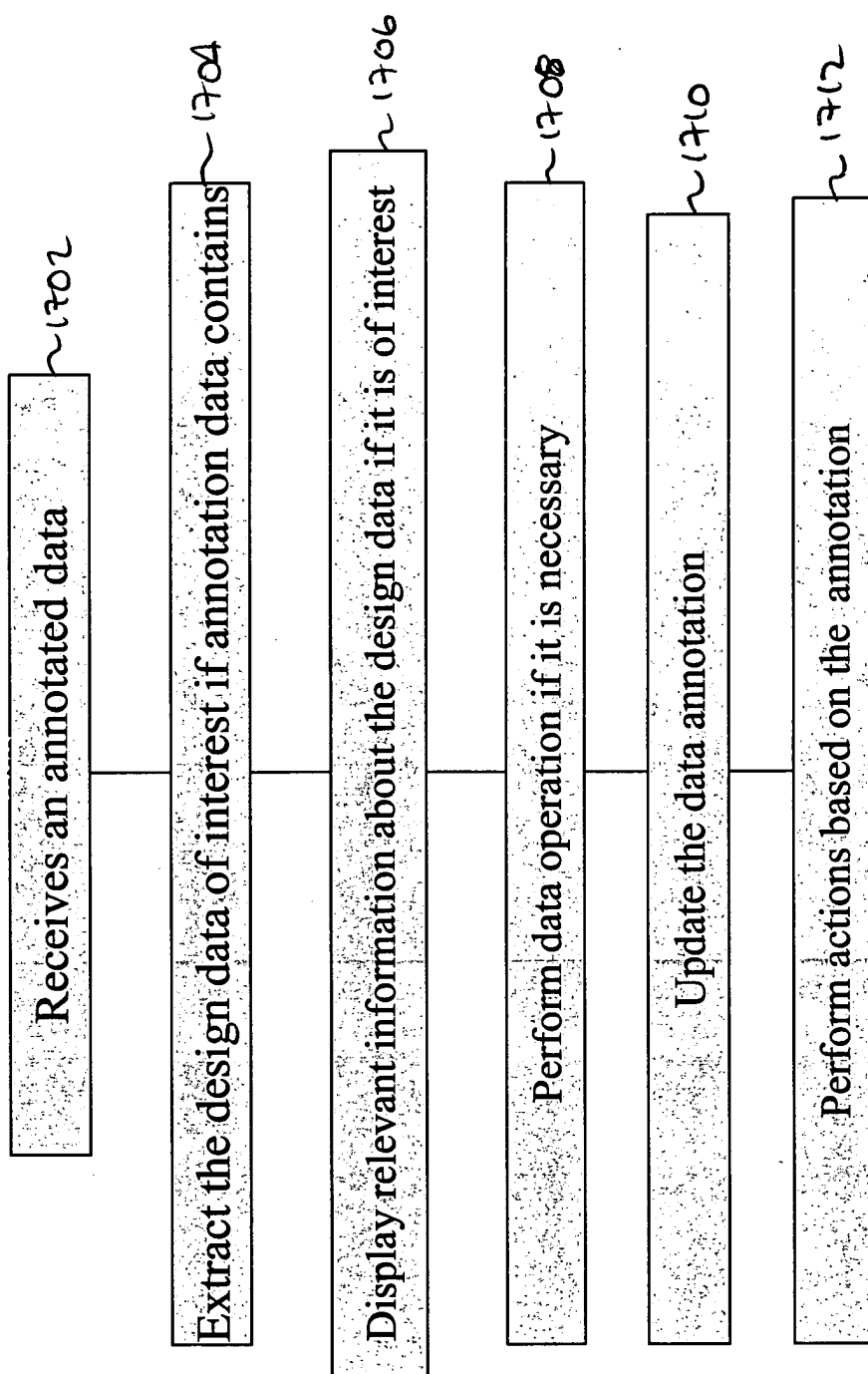
1600
↓

FIG. 16

1760
↓



17/24

FIG. 17

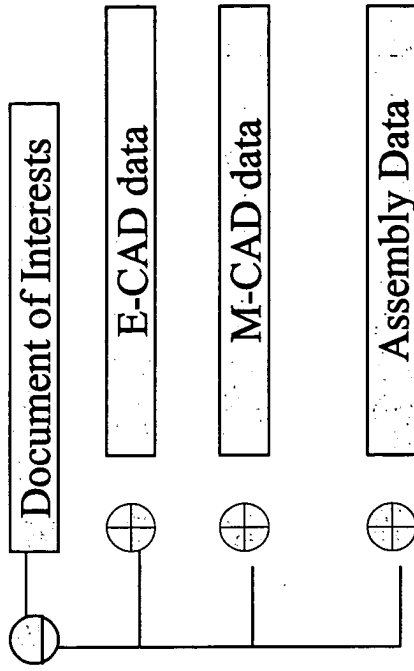


FIG. 18A

18/24

FIG. 18B

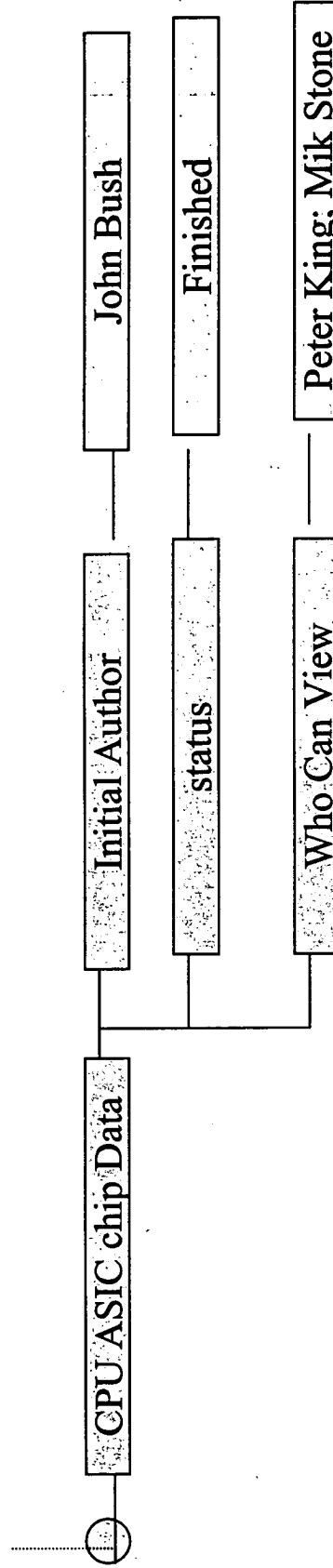


FIG. 18C

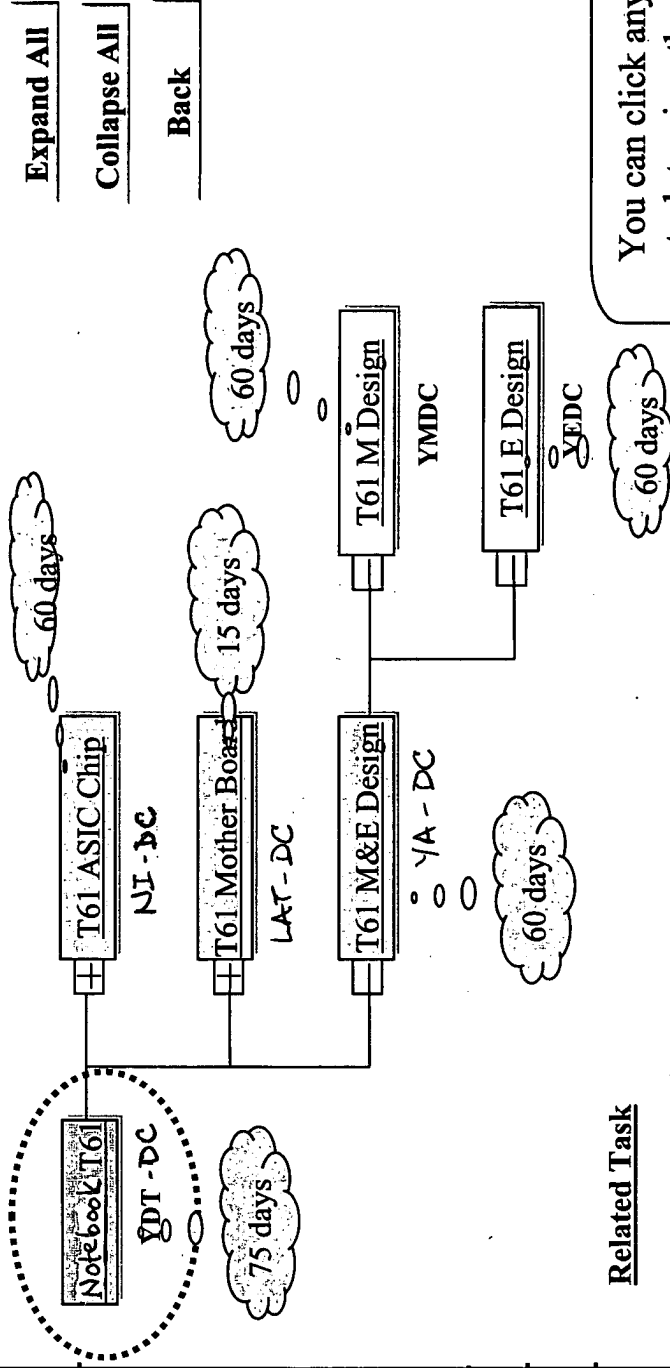
FIG. 19A

YDT-DC Project View

Design Collaboration Portal

<input type="checkbox"/> Project Management <ul style="list-style-type: none">• New Project• List Project• Monitor Project
<input type="checkbox"/> Task Management <ul style="list-style-type: none">• List Task• Monitor Task
<input type="checkbox"/> Process Management <ul style="list-style-type: none">• New Template• Modify Template• Monitor Process
<input type="checkbox"/> Partner Management <ul style="list-style-type: none">• New Partner• Find Partner• List Partner• Modify Partner
<input type="checkbox"/> User Management
<input type="checkbox"/> User Management
<input type="checkbox"/> Sign Out

This page shows the global view of project status.



Related Task

Process Execution View

You can click any task to view the detail information.

FIG. 19B

Top

Pyramid

NOTEBOOK T61

0



75

Bottom

ASIC

0



M Design

60



Mother-Board



75

E Design

Offset Calculation

T61 M Design
YMDC

Offset: $T_{M\ Design} - 60$

T61 E Design
YEDC

Offset: $T_{E\ Design} - 60$

T61 M&E Design
YA-DC

Offset: $\max\{T_{E\ Design} - 60, T_{M\ Design} - 60\}$

T61 Mother Board
LAT-DC

Offset: $\max\{T_{E\ Design} - 60, T_{M\ Design} - 60, T_{ASIC} - 60\} + T_{Board} - 15$

T61 ASIC Chip
NT-DC

Offset: $T_{ASIC} - 60$

Notebook T61
YDT-DC

Offset: $\max\{T_{E\ Design} - 60, T_{M\ Design} - 60, T_{ASIC} - 60\} + T_{Board} - 15$

It must be calculated after all M&E, ASIC

At any time t, if T_{ASIC} etc. will take the value of t for the calculation

Checkpoint Calculation

FIG. 19D

T61 M Design
YMDC

$$T_{M\text{ Design}} - 60 + 60$$

T61 E Design
YEDC

$$T_{E\text{ Design}} - 60 + 60$$

T61 M&E Design
YA - DC

$$\max\{T_{E\text{ Design}} - 60, T_{M\text{ Design}} - 60\} + 60$$

T61 Mother Board
LAT - DC

$$(T_{\text{Board}} - 15) + \max\{T_{E\text{ Design}} - 60, T_{M\text{ Design}} - 60, T_{\text{ASIC}} - 60\} + 60$$

T61 ASIC Chip
NI - DC

$$\text{Offset: } T_{\text{ASIC}} - 60 + 60$$

Note Book T61
YDT - DC

Same as Motherboard

It must be calculated after all M&E, ASIC

At any time t, if T_{ASIC} etc. will take the value of t for the calculation

Fig. 19E

Energy Calculation

$$0.5 * \text{Sign}[\text{CheckPoint} - \text{BaseCheckPoint}] \\ * K \\ * [\text{CheckPoint} - \text{BaseCheckPoint}]^2$$

Here K gives the importance of the process

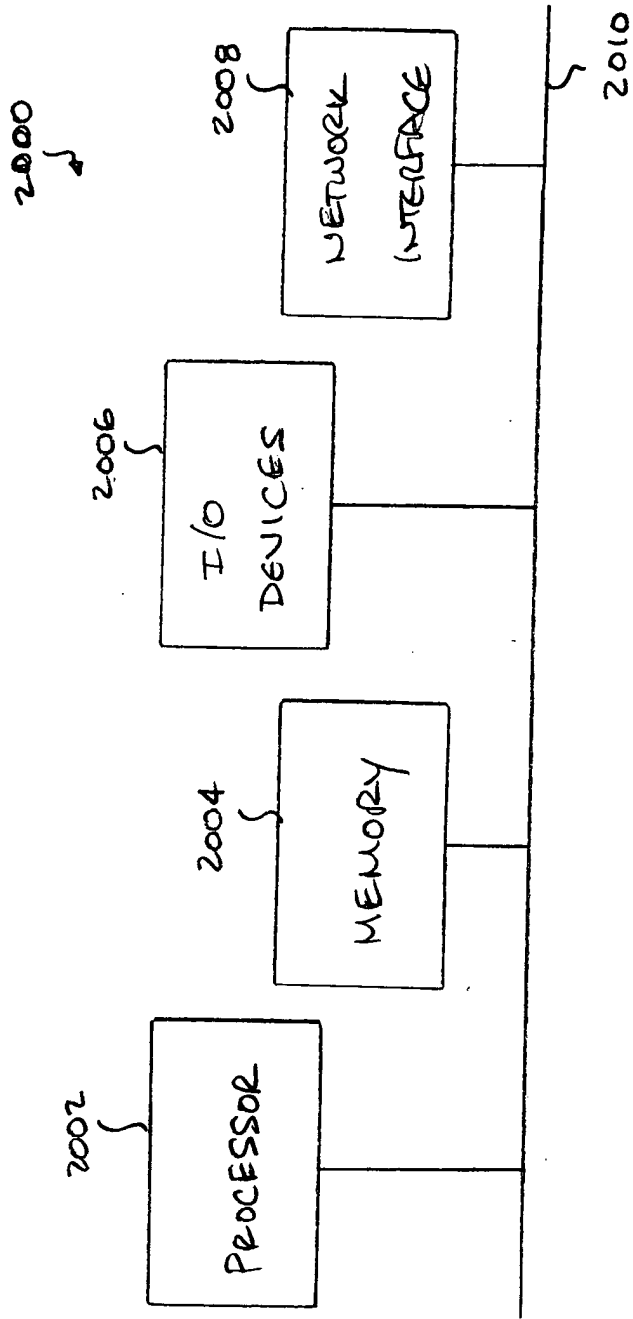


FIG. 20